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EXAMINER	
AMAYA, CARLOS DAVID	
ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 06/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/774,251	NGUYEN, THAT	
	Examiner	Art Unit	
	Carlos Amaya	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-16,20,24-28 and 30* is/are rejected.

7)☐ Claim(s) *6,17-19,21-23 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/06/2004*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 14 is objected to because of the following informalities: It appears that on line 3 of claim 14 the word "and" should be replace with "or". Also the word "Schotky" should be "Schottky" Appropriate correction is required.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Thornton (US 5,027,002).

With respect to claim 1 Thornton discloses a redundant power supply device (Redundant circuit cards) for an electrical system, comprising: a first converting device (Active circuit card 22) configured to convert a first input voltage signal into a primary logic supply voltage signal (Input Voltage Vcc is supplied to the circuit card 22, also a DC-DC converter is located in the card 22, Column 2 lines 55-57); a second converting device (Standby circuit card 24) configured to convert a second input voltage signal into a backup logic supply voltage signal (A signal Vcc is also supplied to the stand by circuit card 24, it also contains a converter, Column 2 lines 55-57); and first and second outputs configured to output the primary and backup logic supply voltage signals,

respectively, to one or more components in the electrical system (Output signal 42 is provided to electrical components, Thornton discloses that the redundant circuit cards are for use in aircraft electrical power systems, thus the output signal must be supplied to electrical systems).

3. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Wood (US 5,726,506).

With respect to claim 1 Wood discloses a redundant power supply device (Power units 1) for an electrical system, comprising: a first converting device (Power Unit A) configured to convert a first input voltage signal into a primary logic supply voltage signal (Power unit A comprises a power supply 6, and it produces two different voltage levels, thus it must inherently have a converting device to provide different power outputs); a second converting device (Power units B and C) configured to convert a second input voltage signal into a backup logic supply voltage signal (Power units B and C are of similar construction as power unit A and must me equipped with a converter); and first and second outputs configured to output the primary and backup logic supply voltage signals, respectively, to one or more components in the electrical system (Output signals are provided to Modules A, B and C via power buses 11, 12 and 13 these buses supply the electrical components).

With respect to claim 2 Wood discloses the redundant power supply device according to claim 1, wherein the components of the electrical system include one or more circuit cards utilizing digital circuitry (Modules A, B and C, Column 4 lines 66-67, Column 5 lines 1-2), and each of the first and second converting devices is configured

to convert a respective input voltage into a logic supply voltage signal that is compatible with logic levels associated with the digital circuitry of each circuit card (Column 3 lines 30-34).

With respect to claim 3 Wood discloses the redundant power supply device according to claim 1, wherein the first and second converting devices are configured so that voltage levels of the primary and backup logic supply voltages are substantially equal to Vcc + Vdiode (Vcc being provided by PS 6, and Vdiode is the "Oring" diode 10 Column 5 lines 29-30), Wherein Vcc is a voltage level associated with a HIGH logic level for digital circuitry in each circuit card, and Vdiode is a voltage drop across an ORing diode in each circuit card (The voltage Vcc is provided to Each module via the Bus 11 and "ORing" diode 10 provided on each of the Power Units).

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1-2, 7-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Beneditz (US 6,856,045).

With respect to claim 1 Beneditz discloses a redundant power supply device (Power distribution assembly) for an electrical system, comprising: a first converting device (Power Modules 30 figure 2) configured to convert a first input voltage signal (Voltage signal from power supply # 1) into a primary logic supply voltage signal (Power supply # 1 supplies the modules 30 and a microprocessor 34); a second converting device (Power Modules 30, function as second converting device) configured to convert a second input voltage signal into a backup logic supply voltage signal (Modules 30 are configured to convert the received voltage, Column 4 lines 17-21); and first and second outputs configured to output the primary and backup logic supply voltage signals, respectively, to one or more components in the electrical system (Column 4 lines 17-21, lines 25-27).

With respect to claim 2 Beneditz discloses the redundant power supply device according to claim 1, wherein the components of the electrical system include one or more circuit cards utilizing digital circuitry (The power modules 30 are utilized in vehicles, such as an aircraft to power various system, thus one would envisioned that the system would power circuit cards), and each of the first and second converting devices is configured to convert a respective input voltage into a logic supply voltage signal that is compatible with logic levels associated with the digital circuitry of each circuit card (Column 4 lines 25-27).

Whit respect to claim 7 Beneditz discloses the redundant power supply device according to claim 1, further comprising: a monitoring device (Microprocessors 34 and 38) configured to output a signal indicating a status of each of the first and second input voltage signals (The microprocessors inherently monitor the signals from the first and second Voltage supply, Column 3 lines 63-67, Column 4 lines 5-12. There is also a multifunction control display unit 74, Figure 7, Column 5 lines 3-7).

With respect to claim 8 Beneditz discloses the redundant power supply device according to claim 1, wherein the second converting device is configured to convert one or more input voltage signals, which are received in addition to the second input voltage signals, into backup logic supply voltage signals that are distributed to the components of the electrical system (As shown in figure 4 the IPS 56 of the power module 30 is able to receive and convert signals from the first and second power supplies).

With respect to claim 9 Beneditz discloses a dual-redundant power supply interface for a circuit card, comprising: a first input node configured to receive a first voltage signal supplied to the circuit card (Figure 4 shows IPS 56 configured to received voltage signals from the First and second power supplies); a second input node configured to receive a second voltage signal supplied to the circuit card; and a fault-tolerance module (Internal power supply (IPS) 56) operably connected to the first and second input nodes, the fault-tolerance device being configured to allocate one of the first and second voltage signals as a logic supply voltage of the circuit card, while the other of the first and second voltage signals remains idle (The microprocessors 34 and

38 control which power supplies is going to power the modules, thus IPS 56 of the power modules 30 detects which signal is active and which signal is on standby).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thornton (US 5,027,002) in view of Wood (US 5,726,506).

With respect to claim 4 Thornton discloses the redundant power supply device according to claim 1, a DC-DC converter operably connected to the signal conditioner to convert the voltage level of the conditioned DC voltage signal, thereby generating a logic supply voltage signal.

Thornton, however, does not disclose expressly that each of the first and second converting devices include a signal conditioner configured to receive an input voltage signal and output a conditioned DC voltage signal.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have added a signal conditioner in the redundant circuit cards disclosed by Wood.

The suggestion or motivation for doing so would have been to provide the DC-DC in the Circuit cards with a Clean DC signal; thus depending upon the received Vcc coming from power source 10 one of ordinary skill in the art would have added a signal conditioner for the purpose of providing a DC signal to the DC-DC converter in the Circuit cards.

With respect to claim 5 Thornton in view of Wood discloses the redundant power supply device according to claim 1, however, they do not disclose expressly that the first and second converting devices are configured so that a voltage level of the primary logic supply voltage signal is higher than a voltage level of the backup logic supply voltage signal. It would have been obvious to one of ordinary skill in the art at time the invention was made to have power supplies with different power ratings, since power supplies could come from batteries, generators or converters their ratings could be different. Thus, it would have been obvious to have power supplies coming from different sources with different ratings.

The suggestion or motivation for doing so would have been to provide a better redundancy in the system, thus increasing the safety and reliability of the system, since power of different ratings and different sources are feeding the system.

8. Claims 10-11,20,24,28,30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beneditz (US 6,856,045)

With respect to claim 10 Beneditz discloses the dual-redundant power supply interface according to claim 9, and that the fault-tolerance module is configured to

allocate the first voltage signal as the logic supply voltage, while the second voltage signal remains idle, however, Beneditz does not disclose expressly that the first voltage signal has a higher voltage level than the second voltage signal.

It would have been obvious to one of ordinary skill in the art at time the invention was made to have power supplies with different power ratings, since power supplies could come from batteries, generators or converters their ratings could be different. Thus, it would have been obvious to have power supplies coming from different sources.

The suggestion or motivation for doing so would have been to provide a better redundancy in the system, thus increasing the safety and reliability of the system.

With respect to claim 11 Beneditz discloses the dual-redundant power supply interface according to claim 10, wherein the fault-tolerance module is configured to allocate the second voltage signal as the logic supply voltage when the first voltage signal becomes disabled (Column 4 lines 7-12).

With respect to claim 20 Beneditz discloses an electrical power distribution system comprising: a power supply device for generating redundant DC supply voltages from a plurality of power sources (Power supplies 42 and 48); redundant power distribution buses operably connected to the power supply device to distribute the redundant DC supply voltages (As shown in figure 4 the voltage from the two power supplies are distributed to the microprocessors and the power modules); and an interface operably connected to the redundant power distribution buses to receive the redundant DC supply voltages, wherein the interface is configured to allocate one of the

redundant DC supply voltages as a logic supply voltage for the digital logic device (The power modules 30 have a IPS 56 that is operable to receive the voltage signals from the two power supplies, Column 4 lines 17-21). However, does not disclose expressly that the power distribution system comprises one or more circuit cards, each including, a digital logic device. Beneditz discloses that the power modules 30 are utilized in vehicles, such as an aircraft to power various system, thus one would envisioned that the system would power circuit cards containing digital logic device; furthermore Beneditz discloses that the power modules are used to control aircraft systems such as braking, navigation, or temperature control systems (See abstract).

The suggestion or motivation for doing so would have been to provide power to systems that operate in response to the voltage input from the power modules; this system are vital to the proper operation of the vehicle, thus if one power supply fails the second power supply is going to take over and supply with power the vital component.

With respect to claim 24 Beneditz discloses the system according to claim 20, wherein the interface includes a fault-tolerance module operably connected to receive the first and second DC supply voltages from the power distribution buses, the fault-tolerance device (IPS 56) being configured to allocate the first DC supply voltage as the logic supply voltage, while allowing the second DC supply voltage to remain idle (The IPS is capable of receiving either of the two voltages signals from the two power supplies). However, Beneditz does not disclose expressly that the first DC supply voltage having a higher voltage level than the second DC supply voltage.

Thus, it would have been obvious to have power supplies coming from different sources with different ratings, one having a higher level than the other.

The suggestion or motivation for doing so would have been to provide a better redundancy in the system, thus increasing the safety and reliability of the system, since power of different ratings and different sources are feeding the system.

With respect to claim 28 Beneditz discloses the system according to claim 24, wherein the fault tolerance module is further configured to allocate the second DC supply voltage as the logic supply voltage when the first DC supply voltage becomes disabled (If the signal from the first supply becomes disable IPS 56 is capable of receiving and allocating the second signal from the second power supply, Column 4 lines 17-21).

With respect to claim 30 Beneditz discloses the system according to claim 20, including a status monitoring module (Microprocessors 34 and 38) configured to output a signal indicating a status of each of the plurality of power sources. (The microprocessors inherently monitor the signals from the first and second Voltage supply, Column 3 lines 63-67, Column 4 lines 5-12. There is also a multifunction control display unit 74, Figure 7, Column 5 lines 3-7)

9. Claims 12-16, 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beneditz (US 6,856,045) in view of Thornton (US 5,027,002).

With respect to claim 12 Beneditz discloses the dual-redundant power supply interface according to claim 10, however, does not disclose expressly that the fault-tolerance module includes two diodes connected in a logical OR configuration.

Thornton discloses "ORing" diodes 16 and 18 of the power source 10 of figure 1.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have included the "ORing" diodes in the Internal power supply (IPS) 56 of Beneditz invention.

The suggestion or motivation for doing so would have been to provide better redundancy when supplying power from two different sources connected to the two diodes, thus power is always provided to the circuitry regardless if one of the power supplies fails.

With respect to claim 13 Beneditz discloses the dual-redundant power supply interface according to claim 12, however, does not disclose expressly that the fault-tolerance module has a configuration including, a first ORing diode whose anode receives the first voltage supply signal, a second ORing diode whose anode receives the second voltage signal, an output node at which the cathodes of the first and second ORing diodes are commonly connected, the output node outputting the logic supply voltage to one or more components of the circuit card.

Thornton, however, discloses the "ORing" diode configuration as claimed above, as can be seen on figure 1 Power source 10.

With respect to claim 14 Beneditz in view of Thornton discloses the dual-redundant power supply interface according to claim 13, however Beneditz nor Thornton do not disclose that a fuse is connected in series with at least one of the first or second ORing diodes.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have included fuses in series with the diodes, for the purpose of providing protection to the circuitry.

With respect to claim 15 Beneditz in view of Thornton discloses the dual-redundant power supply interface according to claim 13, however, Beneditz nor Thornton disclose that the first and second ORing diodes are Schottky diodes. One of ordinary skill in the art would have necessarily used any type of diodes depending on the design parameters and the desired output result.

With respect to claim 16 Beneditz in view of Thornton discloses the dual-redundant power supply interface according to claim 15, however, they do not disclose expressly that at lest one of the components of the circuit card is a digital logic device. The power modules 30 are utilized in vehicles, such as an aircraft to power various system, thus one would envisioned that the system would power circuit cards containing digital logic devices.

With respect to claim 25 Beneditz discloses the system according to claim 24, however, Beneditz do not disclose expressly that the fault tolerance module includes two diodes in a logical OR configuration.

Thornton discloses "ORing" diodes 16 and 18 of the power source 10 of figure 1.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have included the "ORing" diodes in the Internal power supply (IPS) 56 of Beneditz invention.

The suggestion or motivation for doing so would have been to provide better redundancy when supplying power from two different sources connected to the two diodes, thus power is always provided to the circuitry regardless if one of the power supplies fails.

With respect to claim 26 Beneditz in view of Thornton discloses the system according to claim 25, however, they do not disclose expressly that the interface further comprises: a fail-safe mechanism operable to protect the first and second DC supply voltages when a short circuit occurs in the diodes of the logical OR configuration, the fail-safe mechanism including a fuse connected in series with each of the diodes, respectively.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have included fuses in series with the diodes, for the purpose of providing protection to the circuitry. As it is a standard procedure to provide fuses to protect circuitry.

With respect to claim 27 Beneditz in view of Thornton discloses the system according to claim 25, however, they do not disclose expressly that the diodes are Schottky ORing diodes

One of ordinary skill in the art would have necessarily used any type of diodes depending on the design parameters and the desired output result.

Allowable Subject Matter

10. Claims 6, 17-19, 21-23, 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. Claim 6 is allowable over the prior art of record, because the prior art of record do not suggest "the first input voltage signal is an AC voltage signal and the second input voltage signal is a DC voltage signal, and the signal conditioner of the first converting device includes an auto-ranging rectifier and filter".

12. Claim 17 is allowable over the prior art of record, because the prior art of record do not suggest "that the circuit card includes digital circuitry, each of the first and second voltage signals being a DC signal whose voltage level is compatible with logic levels associated with the digital circuitry, and the dual-redundant power supply interface further comprises: one or more converters operably connected to the fault-tolerance module to receive the logic supply voltage, each converter being configured to convert the logic supply voltage and deliver the converted logic supply voltage to an operably connected component of the circuit card".

13. Claims 18-19 are allowable since they depend on allowable claims.

14. Claim 21 is allowable over the prior art of record, because the prior art of record do not suggest "a first converting device configured to condition and convert a first input voltage signal into a primary logic supply voltage; a second converting device configured to condition and convert a second input voltage signal into a backup logic supply voltage, wherein the primary and backup logic supply voltages have voltage

levels compatible with the logic levels associated with the digital logic device, the voltage level of the primary logic supply voltage being higher than the voltage level of the backup logic supply voltage".

15. Claims 22 and 23 are allowable since they depend on allowable claims.

16. Claim 29 is allowable over the prior art of record, because the prior art of record do not suggest "one or more DC-DC converters operably connected to the fault tolerance module to receive the allocated logic supply voltage, each DC- DC converter being configured to deliver a converted DC power source voltage lo a corresponding one of the SSPCS". Along with the remaining parts of the claim.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to the examiner's supervisor, Brian Sircus can be reached on (571)272-2800. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CA

Stephen W Jackson
6.20.06

STEPHEN W. JACKSON
PRIMARY EXAMINER